Quest Journals
Journal of Electronics and Communication Engineering Research
Volume 8 ~ Issue 7 (2022) pp: 06-16
ISSN(Online) : 2321-5941
www.questjournals.org

Research Paper

Design and Investigation the characteristics of BFW 10 n Channel JFET Single Stage Negative Voltage Feedback Transistor Amplifier

[1]Abdullahi, Y., 2 Sahabi, B.B., A.A. [3]Sifawa, and [4]Yahaya, Z.
[1, 2] *Department of Science Laboratory Technology, Umaru Ali Shinkafi Polytechnic Sokoto, Nigeria*
[3, 4] *Department of Physics, Sokoto State University, Sokoto, Nigeria*

Abstract
A practical amplifier has a high gain as a result of even a careless disturbance at the input will appear in the amplified form in the output, because of that there is a strong tendency in amplifier to introduce a noise due to sudden temperature changes or wandering electric and magnetic fields. The noise in the output of an amplifier is undesirable and must be kept to a small level as possible; this noise level in amplifier can be reduced considerably by the use of negative feedback. In this paper, amplifier with and without negative voltage feedback using BFW 10 n channel JFET single stage was designed, analyzed and the results of the two amplifiers compared characterized BFW 10 n channel JFET single stage with negative voltage feedback amplifier with low level gain of 10.88db to 6.02db, has the advantages of increased in bandwidth from 10Hz to 1MHz, controls in distortion, higher input impedance of 789.495kΩ to 0.172 kΩ and lower output impedance 2.220018 kΩ to 11.642123 kΩ as compared to the one without the feedback using Multisim 14.2 simulator .
Keywords: *Amplifier, Analysis, BFW 10 n Channel JFET, Single Stage, Feedback*

*Received 01 July, 2022; Revised 10 July, 2022; Accepted 12 July, 2022 © The author(s) 2022. Published with open access at **www.questjournals.org***

I. Introduction

A Negative-feedback amplifier is an electronic amplifier that subtracts a fraction of its output from its input, so that negative feedback opposes the original signal (Experts, 2019). The different types of feedback amplifiers are: Voltage Series, Voltage Shunt, Current Series and Current Shunt (Rao, 2012). It can be applied in regulating power supply, where a large bandwidth is required and in various amplifiers' design of the electronics field (Piguet, 2018). Some of the properties are: Disturbance rejection, sensitivity, dynamic tracking, steady-state error, and stability (Franklin *et al*., 2015).

Many authors carried out researchers on Feedback amplifier using different simulators software packages, some of them are: Singh & Mehra, (2018) carried out a research on Qualitative Analysis of Darlington Feedback Amplifier at 45nm Technology, the comparison of single stage and three stage feedback Darlington feedback amplifier with reference to gain, bandwidth and swing rate was simulated on cadence analog design environment at GPDK 45nm technology, the results shows that increase in gain, bandwidth and swing rate of three stage Darlington feedback amplifier can show better stability over the single stage Darlington feedback amplifier.

Sikder & Ali,(2021) carried out a research on Performance analysis of High Frequency Class E Feedback amplifier with Schmitt Trigger driver, the simulated performance analysis of class E amplifier along with sine wave to square wave converting driver was done in Cadence Virtuoso 6.1.5 with Spectre simulator using 280nm gpdk090 technology, the resultant design yielded power gain of 11.41dB and producing an output power of 15.78dBm. It also had IIP3 of 3.697 with 57% efficiency which is high efficiency.

Zanjani *et al*.,(2018) carried out a research on High-precision, resistor less gas pressure sensor and instrumentation amplifier in CNT technology, a new high precision, pressure sensor for sensing gas molecules using a controllable voltage-mode instrumentation amplifier (VMIA) in carbon nanotube field-effect transistor (CNTFET) technology was designed, the sensing mechanism was simulated in ANSYS which justifies the variations of sensing capacitance, while the sensor's output voltage was applied to an accurate instrumentation amplifier (IA) via a switched-capacitor sensor driver.

Fuada *et al*,. (2016) carried out a research on Trans-Impedance Amplifier (TIA) design for Visible Light Communication (VLC) using commercially available OP-AMP, the empirical experiment of TIA for high-band VLC with over 1-MHz Gain Bandwidth Product (GPWP) was estimated, selection of the best resistor feedback (Rf) and compensator (Cf) were presented and Comparison of simulation approach against real implementation of OP-AMP chosen from Texas Instruments product, OPA 656 were presented using TINA SPICE simulator. However some of the simulators have difficulties for beginners in that case Multisim can be used for simplicity and acceptable accuracy. The paper came up with a Design and Analysis of BFW 10 n Channel JFET Single Stage Feedback Amplifier with Low-level Gain, Increased in Bandwidth, Controls in Distortion, Higher Input Impedance and Lower Output Impedance using Multisim 14.2 simulator.

II. Design

An amplifier in which feedback is incorporated known as feedback amplifier (Navas & Suhail, 2010). The block diagram of typical feedback amplifier with a gain A_V, mixer network, sampling network and a feedback network shown in Figure1.

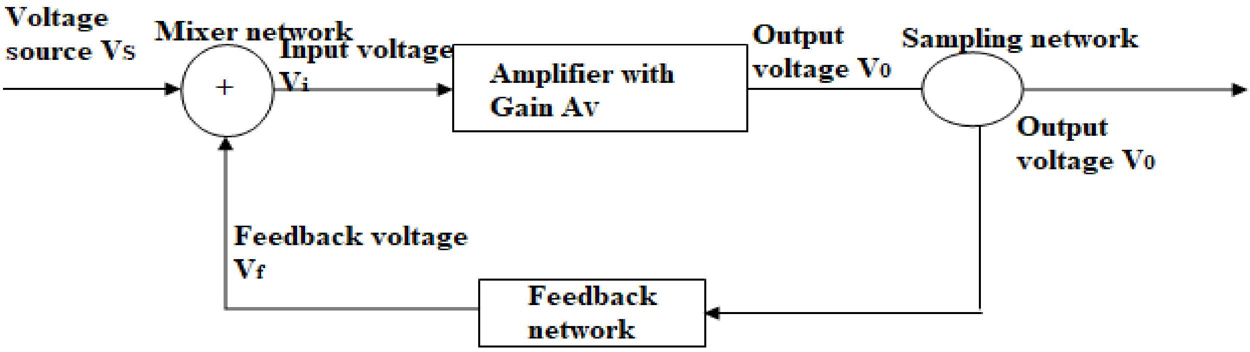

Figure1: Block Diagram of Feedback Amplifier

2.1. Design Negative Voltage Feedback Amplifier using BFW 10 n channel JFET

To design negative voltage series feedback common source amplifier using BFW 10 JFET at the desired voltage drop, the value R_D and R_S can be calculated through the following expression:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2 \qquad (1)$$

$$V_{DD} = I_D R_D + V_D$$

$$\therefore R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(10-5)V}{3.4095\,mA} = 1.47k\Omega \qquad (2)$$

Since the simulated results of BFW 10 n channel JFET at gate shorted condition ($V_{GS} = 0$) from figure 9 are: $I_D = I_{DSS}\,(max) = 6.819mA$, and $V_{DS} = V_{DD\,(max)} = 10V$, also the drain current and voltage at midpoint is $I_D = I_{DSS}/2$ and $V_D = V_{DD}/2$ respectively and $V_{GS\,(Off)} = -V_P = -3.5V$, these are the operating point for d.c circuit condition of the amplifier (Mehta &Mehta, 2008).

Where;

$V_{DD} = V_{DS\,(max)} =$ Maximum drain source voltage at $V_{GS} = 0V$

$R_D =$ Drain resistance

$I_D =$ drain current at given V_{GS}

$I_{DSS} =$ shorted gate drain current

$V_{GS} =$ gate source voltage

Negative pinch off voltage $(-V_P) =$ gate source cut off voltage $V_{GS\,(off)}$ (Meh & Mehta, 2008).

And

$$V_G = V_{GS} + V_S$$

$$V_S = V_G - V_{GS}\,, \qquad (3)$$

But $V_G = 0$, at shorted gate condition, $V_S = I_D R_S$ and substituting the values of $I_D = 3.409mA$, $I_{DSS} = 6.819mA$ and $V_{GS\,(off)} = -3.5V$ from figure 9 into equation one, we have

$$V_{GS} = -1.0256V$$

$$\therefore R_S = \frac{V_S}{I_D} = \frac{1.0256\,V}{3.409\,mA} = 0.30k\Omega \qquad (4)$$

Where;

$R_S =$ Source resistance

$V_G =$ Gate voltage

V_{GS} = Gate source voltage
V_S = Source voltage
Also with voltage divider bias R_1 and R_2 can be calculated as follows
$V_{DD} = I_1R_1 + V_G$
$R_1 = \frac{V_{DD} - V_G}{I_1}$ but $I_1 = I_2$
$R_1 = \frac{V_{DD} - V_G}{I_2}$ and $V_2 = I_2R_2 = V_G$
$I_2 = \frac{V_G}{R_2} = \frac{2.0483\,V}{1M\Omega} = 0.000002048 = 2.048\mu A, R_1 = \frac{(10 - 2.0483)V}{2.048\,\mu A} = 3.882666M\Omega,$
Where ;
$V_G = V_{GS} + V_S = 1.0256 + 3.409mA \times 0.30k\Omega = 2.0483V$ and R_2 $1M\Omega$ usually selected
$\therefore R_1 = 3.882666M\Omega$ and $R_2 = 1M\Omega$ (5)

These are the d.c equivalent circuit which will determine the operating point (d.c. bias levels) for the circuit, while in an a.c equivalent circuit which determines the output voltage and hence voltage gain of the circuit. Here the designer intentionally selects capacitors that are large enough to appear as short circuit to the a.c signal (Mehta &Mehta, 2008). In this case an electrolytic capacitor C_{in} ($\approx$ 10uf) is used to couple the signal to the base of the transistor, a source by pass capacitor C_S($\approx$ 100μf) is used in parallel with R_S to provide a low reactance path to the amplified a.c signal and a coupling capacitor C_c($\approx$ 10μf) couples one stage of amplification to the next stage. The complete JFET amplifier circuit with voltage divider biasing of BFW 10 n-channel common source configuration transistor without feedback is shown in figure 2.

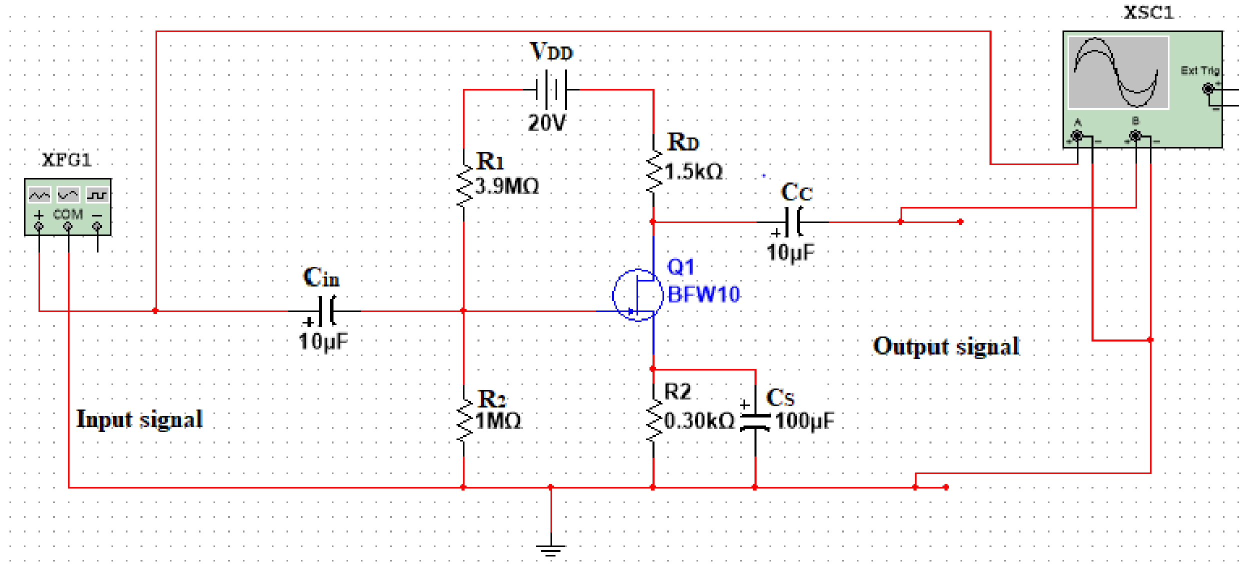

Figure 2: BFW 10 n channel common source configuration transistor amplifier without feedback

The feedback circuit is essentially potential divider consisting of resistances R_1 and R_2 which gives the feedback voltage to the input, it is clear that;
Voltage across $R_1 = \left(\frac{R_1}{R_1 + R_2}\right) \square_0$ (6)
Feedback fraction, $m_v = \frac{\text{Voltage across } R_1}{\square_0} = \frac{R_1}{R_1 + R_2}$ (7)
Where;
$\square_0$ = the output voltage of the amplifier (Mehta &Mehta, 2008).
For this design in under to have feedback fraction of 0.1 R_3 and R_4 are selected as 2kΩ and 18kΩ respectively. The complete JFET amplifier circuit with voltage divider biasing of BFW 10 n-channel common source configuration transistor with feedback circuit is shown in figure 3.

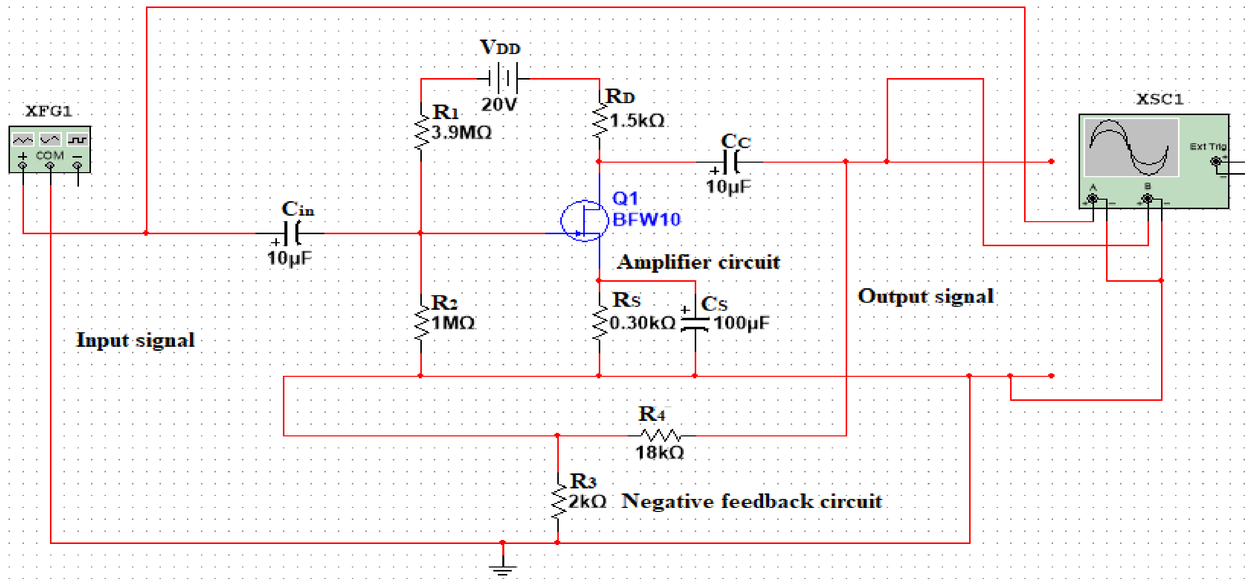

Figure 3: BFW 10 n channel common source configuration transistor amplifier with negative voltage feedback circuit

2.2. Gain of Negative Voltage Feedback Amplifier

Considering the negative voltage feedback amplifier, the output (e_0) must be equal to the input voltage ($e_g - m_v e_0$) multiplied by gain A_v of the amplifier i.e. (Mehta &Mehta, 2008).

$(e_g - m_v e_0)A_v = e_0$

$e_0(1 + A_v m_v) = A_v e_g$

$$\frac{e_0}{e_g} = \frac{A_v}{(1+A_v m_v)} \qquad (6)$$

Where;

$(e_g - m_v e_0)A_v$ = input voltage

e_0 = output voltage

A_v = voltage gain of the amplifier without feedback

$\frac{e_0}{e_g}$ = voltage gain with negative feedback (A_{vf})

$$\therefore\ A_{vf} = \frac{A_v}{(1+A_v m_v)} \qquad (7)$$

It may be seen that the gain of the amplifier without feedback is A_v when negative voltage feedback is applied, the gain is reduced by a factor$(1 + A_v m_v)$.

2.3. Input and Output impedance of CE amplifier with and without negative voltage feedback

The input impedance of an amplifier with and without negative voltage feedback can be calculated using the ac equivalent circuit of the amplifier as follows:

Input impedance without voltage feedback is by

$$Z_{in} = R_1//R_2//Z_{in}(\text{base}) = \frac{R_1 R_2 Z_{in}(\text{base})}{R_2 Z_{in}(\text{base}) + R_2 Z_{in}(\text{base}) + R_1 R_2} \qquad (8)$$

Where;

$Z_{in}(\text{base}) = \beta r'_S,\ \beta = \frac{i_D}{i_G},\ r'_S = \frac{25\text{mV}}{I_S}, I_S \approx I_D$

Z_{in} = Input impedence with feedback

$Z_{in}(\text{base})$ = input impedance of transistor base

β = current gain

r'_S = a.c. source resistance

I_S = d.c. source current

I_D = d.c drain current

Input impedance of the amplifier with negative voltage feedback is give by

$$Z'_{in} = Z_{in}(1 + A_V m_V) \qquad (9)$$

Where;

Z''_{in} = input impedance of the amplifier with negative voltage feedback

Z_{in} = input impedance of the amplifier without negative voltage feedback

A_V = gain without feedback
m_V = feedback fraction
It can be proved that the output impedance (Z_{out}) without negative feedback is given by:

$$Z_{out} = R_E // \left(r_s' + \frac{R_{in}'}{\beta}\right)$$

In practical circuits the value of R_E is large enough to be ignored for this reason the output impedance of the emitter is approximately given by

$$Z_{out} = r_s'' + \frac{R_{in}''}{\beta} \qquad (10)$$

Where;
$R_{in}'' = R_1 // R_2 // R_s$
R_s = resistance connecting before the amplifier input voltage source
$r_s'' = \frac{25\,mV}{I_S}$ = a.c. source resistance
$\beta = \frac{i_{DS}}{i_{GS}}$ = current gain

Output impedance with negative voltage feedback is given by:

$$Z_{out}' = \frac{Z_{out}}{1 + A_V m_V} \qquad (11)$$

Where;
Z_{out}' = output impedance with negative voltage feedback
Z_{out} = output impedance without feedback
The d.c I_S and a.c r_s' can be calculated as follows:
d.c voltage across $R_2, V_2 = \frac{V_{cc}}{R_1 + R_2} \times R_2 = \frac{20}{3.9M\Omega + 1M\Omega} \times 1M\Omega = 4.08V$
d.c voltage across $R_S, V_S = V_2 - V_{BE} = 4.08 - 0.7V = 3.38V$
d.c source current $I_S = \frac{V_S}{R_S} = \frac{3.38}{0.30k\Omega} = 11.27mA$
a.c source resistance $r_S'' = \frac{25mV}{I_S} = \frac{25mV}{11.27mA} = 2.22\Omega$

III. Simulation performance

3.1 Determinations of $I_{DSS}, V_{GS(off)}(-V_p)$ at shorted gate condition

The values of I_{DSS} and $V_{GS\,(off)}(-V_p)$ for BFW 10 n- channel JFET were determined, the proposed simulation circuit diagram at shorted gate condition is shown in Figure 4.

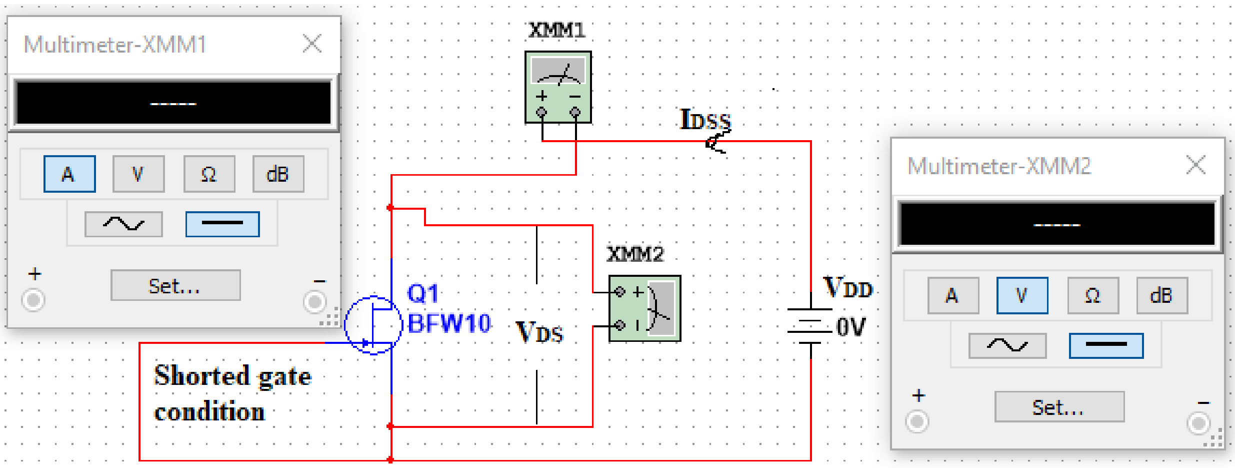

Figure 4: The simulation circuit diagram BFW 10 n- channel JFET with common source at shorted gate condition

3.2. Effect of negative feedback on bandwidth, voltage gain and distortion of BFW10 transistor amplifier

At V_{in} = 10mV and V_{DD} = +20V varying the frequency of the input signal, the gain of the amplifier without and with negative feedback were recorded and the effect of negative feedback on bandwidth, voltage gain and distortion of the amplifier were determined, the proposed simulation circuit diagrams of amplifier without and with feedback circuit are shown in figure 5 and 6.

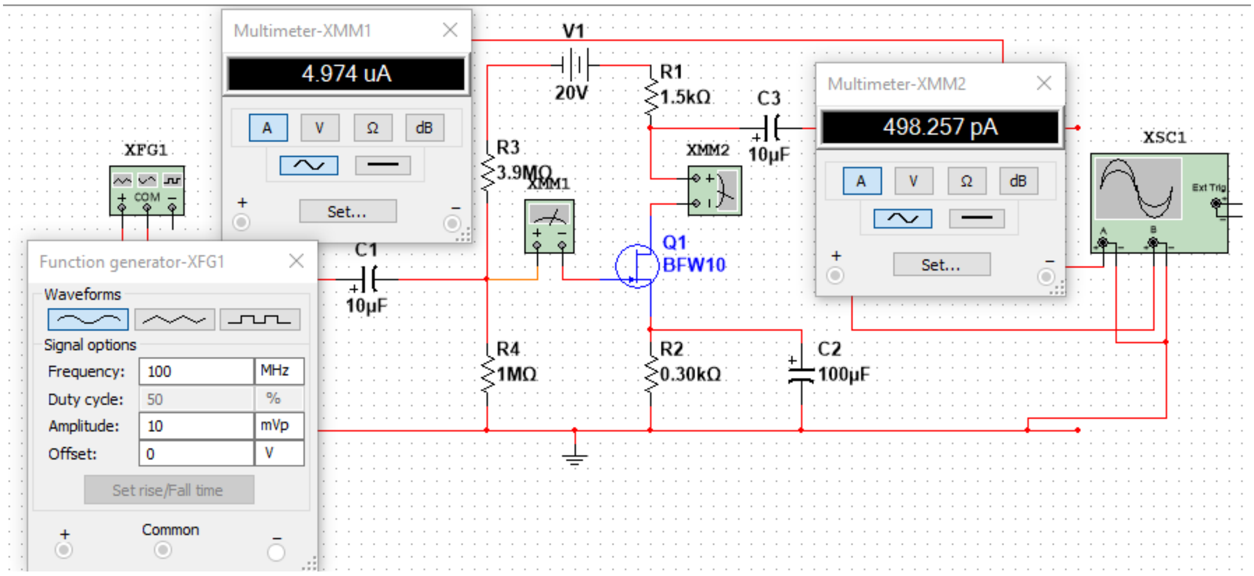

Figure 5: Amplifier without negative feedback circuit

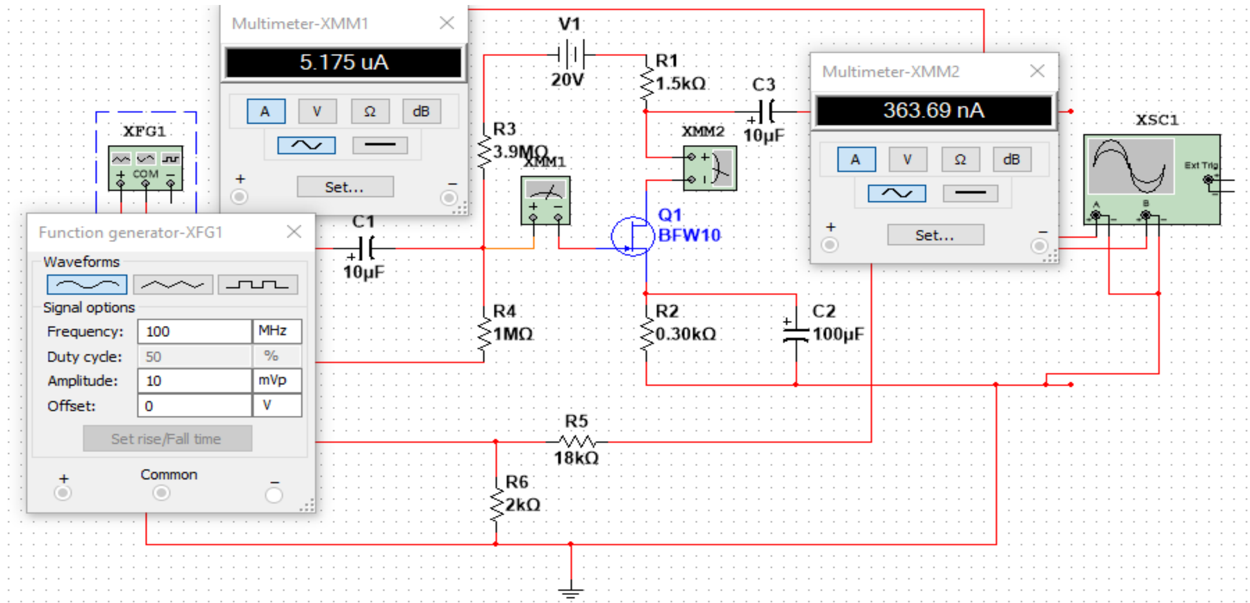

Figure 6: Amplifier with negative feedback circuit

3.3. Effect of negative feedback on gate current(I_{GS}), drain source current (I_{DS}), current gain(β), input impedance of transistor base(Z_{in}(base)), and input impedance of BFW 10 transistor amplifier

At $V_{in} = 10mV$ and $V_{DD} = +20V$ varying frequency of the input signal the effect of negative feedback on gate current(I_{GS}), drain source current (I_{DS}), current gain (β), input impedance of transistor base(Z_{in}(base)), and input impedance of BFW 10 transistor amplifier were determined**,** the proposed simulation circuit diagrams of amplifier without and with feedback circuit are shown in figure 5 and 6.

3.4. Effect of negative feedback on output impedance of BFW 10 transistor amplifier

At $V_{in} = 10mV$ and $V_{DD} = +20V$ varying the frequency of the input signal, the effect of negative feedback on output impedance of BFW 10 transistor amplifier were determined**,** the proposed simulation circuit diagrams with resistance $R_S = 1k\Omega$ connected before the input voltage source of amplifier without and with feedback circuit are shown in figure 7 and 8.

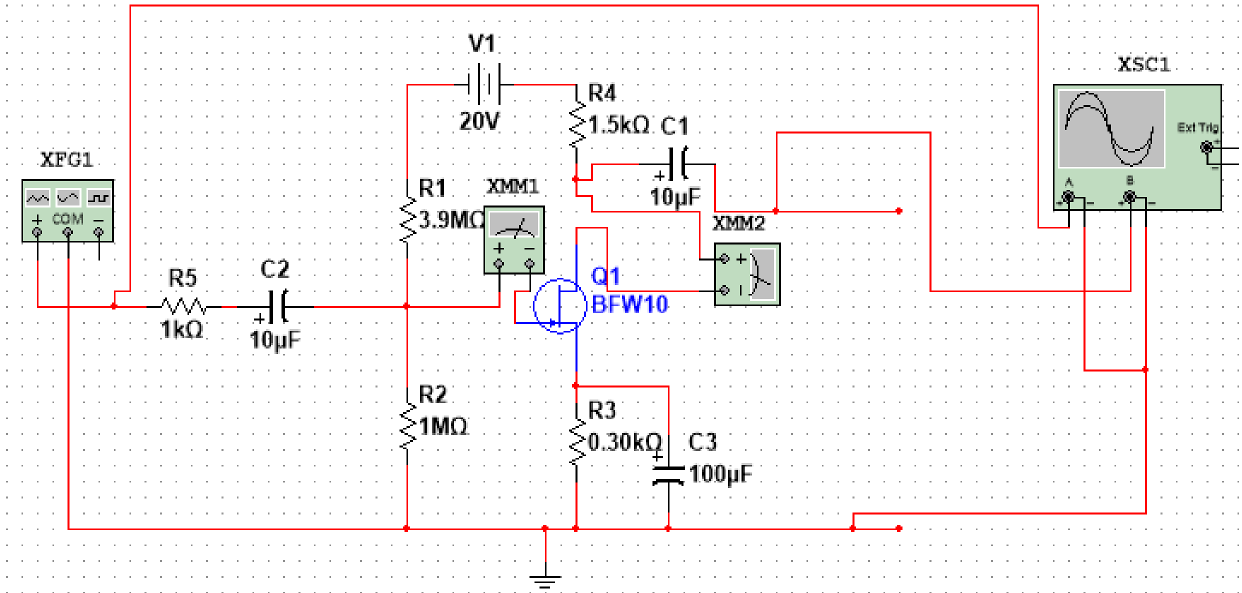

Figure 7: Resistance R_S connected to the amplifier without negative feedback circuit

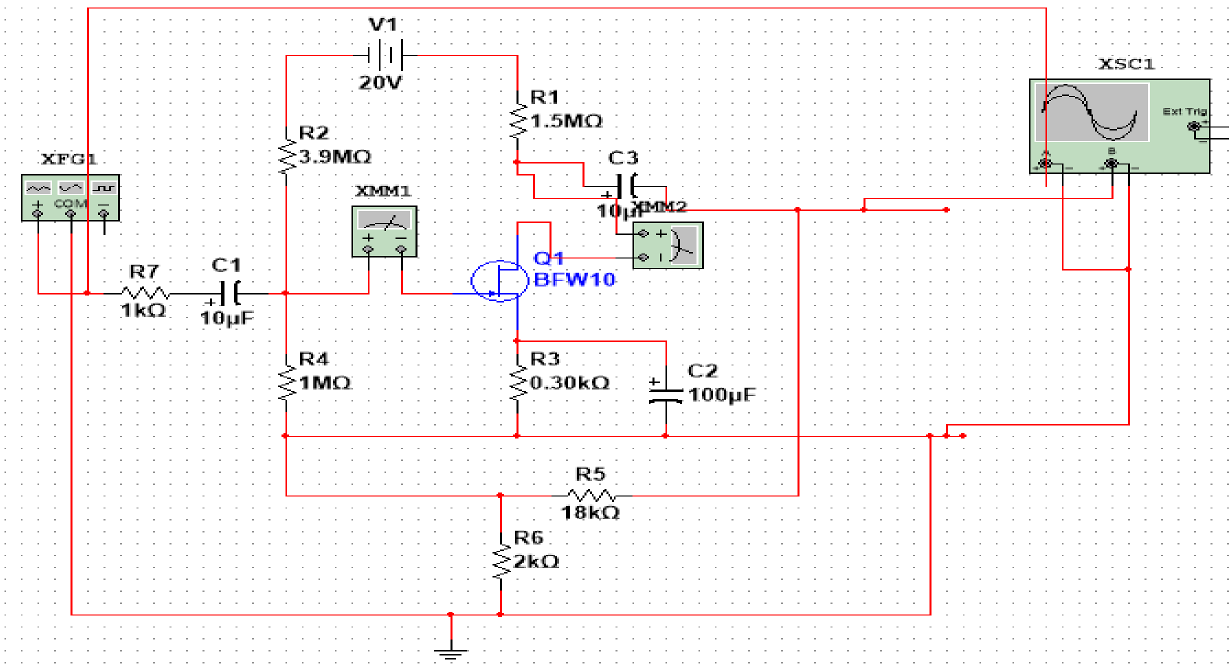

Figure 8: Resistance R_S connected to amplifier with negative feedback circuit

IV. Results Analysis

4.1 The I_{DSS}, $V_{GS(off)}(-V_p)$ results at shorted gate condition

At shorted gate condition varying the drain voltages (V_{DD}) from 0.25, 0.5, 0.75, 1 to 10V the corresponding values of drain current (I_D) and drain source voltage (V_{DS}) were obtained, the graph of (I_D)against (V_{DS}) was plotted, the shorted gate drain current (I_{DSS}), pinch off voltage (V_p) and gate source cut off voltage ($V_{GS\,(off)} = -V_P$) were determined graphically as shown in Figure 9.

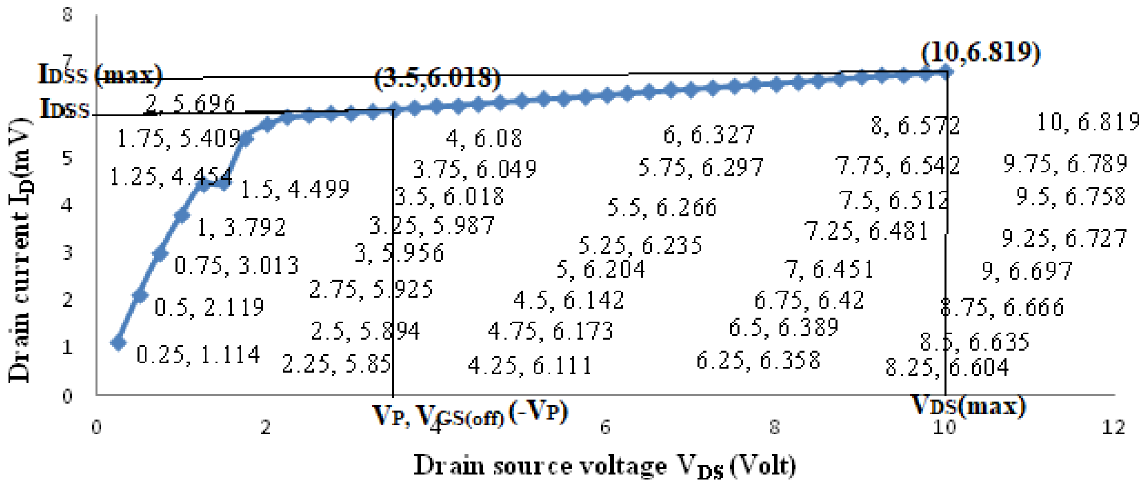

Figure 9: Relationship of Drain current with Drain source voltage

Looking from the graph of figure 9, the maximum shorted gate drain current (I_{DSS}) which have been measured under shorted gate condition is 6.819 mA at 10V maximum drain source voltage ($V_{DS(max)}$), the minimum drain source voltage at which the drain current becomes almost constant is 3.5V this is the pinch off voltage (V_P) therefore gate source cut off voltage ($V_{GS(off)}$) is -3.5V, since the two values are always equal and opposite, the region between V_P and $V_{DS(max)}$ is called constant current or saturation region as long as V_{DS} is kept within this range the I_D will remain almost constant for a constant value of V_{GS}.

4.2. Effect of negative feedback on bandwidth, voltage gain and distortion of BFW 10 transistor amplifier

At operating signals frequencies of 10Hz, 100Hz 200Hz, 500 Hz, 1 KHz, 10 KHz, 1MHz, 10 MHz, 20 MHz, 50 MHz and 100MHz, and constant input voltage of 10V the corresponding output voltages were recorded and voltage gains of the amplifier without and with negative feedback were calculated as shown in table 1.

Table1: Voltage gains of the amplifier without and with negative feedback

Operating signal frequency	V_{in} (mV)	V_{out} (mV) without negative feedback	Voltage gain (A_V) = $\left(\frac{V_{out}}{V_{in}}\right)$ without negative feedback	V_{out} (mV) with negative feedback	Voltage gain (A_{Vf}) = $\left(\frac{V_{out}}{V_{in}}\right)$ with negative feedback
10Hz	10	7500	750	35	3.5
100Hz	10	7500	750	35	3.5
200Hz	10	7500	750	35	3.5
500Hz	10	7500	750	35	3.5
1KHz	10	7500	750	35	3.5
10KHz	10	7500	750	35	3.5
100KHz	10	5000	500	35	3.5
1MHz	10	750	75	35	3.5
10MHz	10	62.5	6.25	30	3.0
20MHz	10	31.3	3.13	25	2.5
50MHz	10	18.8	1.88	23	2.3
100MHz	10	18	1.8	20	2.0

Looking at the data point from the top to down in both column and row of table1, the voltage gains of the amplifier without feedback are largely constant over a wide range of signal with higher power gain and bandwidth from the frequency of 10 Hz to the frequency 10 kHz, but applying negative feedback causes the disadvantage of reduced power gain which make up by the advantage of increased bandwidth to 1 MHz as shown in figure 10, this shows that a very large input voltage will results in amplifier distortion but applying negative voltage feedback will tends to oppose the increase in amplification and maintains it stable or accurately in fixed value which controls the distortion by reducing the output voltage.

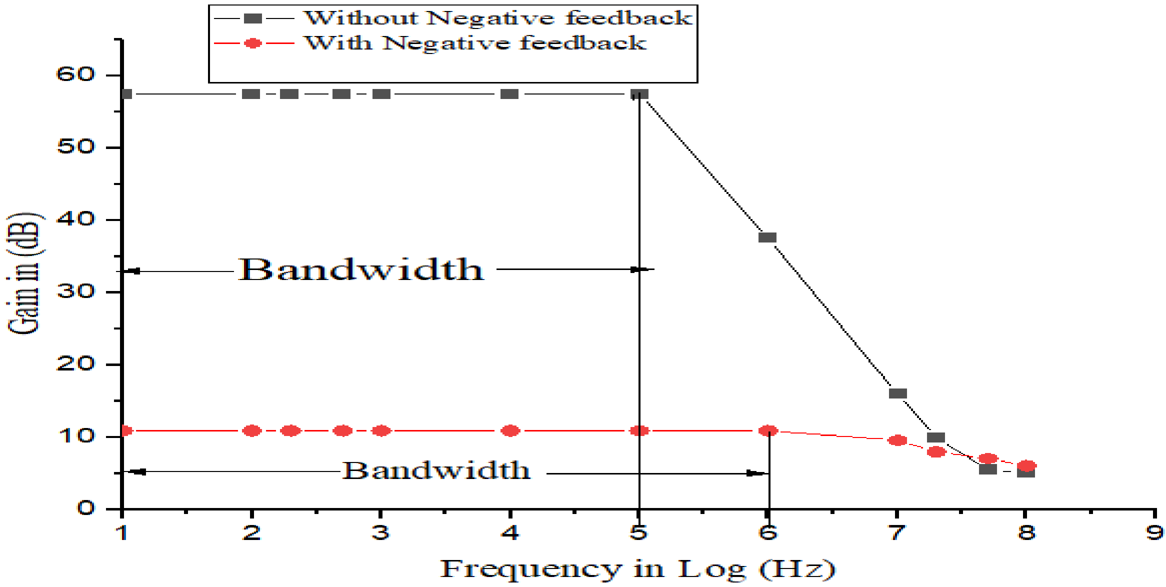

Figure 10: Differences in Bandwidth of amplifier with and without feedback

4.3. Effect of negative feedback on gate current(I_{GS}), drain source current (I_{DS}), current gain (β), input impedance of transistor base(Z_{in}(base)), and input impedance of BFW 10 transistor amplifier

At operating signals frequency of 10 Hz, 100 Hz 200 Hz, 500 Hz, 1 KHz, 10 KHz, 1 MHz, 10 MHz, 20 MHz, 50 MHz, and 100 MHz, the effect of negative feedback on I_{GS}, I_{DS}, β , Z_{in} (base) and input impedance of BFW 10 transistor amplifier were calculated as shown in table 2 and 3.

Table 2: I_{GS}, I_{DS}, β , Z_{in} (base) and input impedance calculated results of BFW 10 transistor amplifier without feedback

Operating signal frequencies	Gate source current (i_{GS})nA	Drain source current (i_{DS})nA	Current gain ($\beta = \frac{i_{DS}}{i_{GS}}$)	Z_{in} (base) $= \beta r_e'$	Input impedance (Zin)kΩ
10Hz	0.103222	640.673	6206.749	137789.983	791.347
100Hz	1.034	652.207	630.761	1400.267	507.470
200Hz	2.043	653.192	319.722	699.466	372.290
500Hz	5.169	653.072	126.344	280.484	207.397
1kHz	10.355	653.208	63.081	140.0398	119.087
10kHz	102.779	648.126	6.306	13.9993	13.757
100kHz	619.13	393.42	0.635	1.4097	1.407
1MHz	772.92	49.151	0.064	0.1421	0.142
10MHz	916.487	5.229	0.0057	0.0127	0.0127
20MHz	1251	2.621	0.002085	0.004629	0.00462349
50MHz	2576	1.282	0.000498	0.00110556	0.001105558
100MHz	4974	0.624	0.00012545	0.000056509	0.000056508

Table 3: I_{GS}, I_{DS}, β , Z_{in} (base)and input impedance calculated results of BFW 10 transistor amplifier with feedback

Operating signal frequencies	Gate source current (i_{GS})nA	Drain source current (i_{DS})nA	Current gain ($\beta = \frac{i_{DS}}{i_{GS}}$)	Z_{in} (base) $= \beta r_e'$	Input impedance (Z_{in}')kΩ
10Hz	0.016725	736.974	44064.2153	97822.558	789.495
100Hz	0.02955	744.72	25202.0301	55948.507	784.755
200Hz	0.041321	745.725	18047.1189	40064.604	780.415
500Hz	0.076049	746.158	9811.5426	21781.625	767.860
I kHz	0.150735	746.882	4954.9341	10999.954	742.214
10kHz	1.449	746.374	515.09312	1143.507	469.282
100kHz	14.472	746.366	51.5731	114.492	100.094
IMHz	144.143	744.319	5.1637	11.463	11.300

10MHz	1152	624.972	0.5425	1.204	1.202
20MHz	1706	510.707	0.2994	0.665	0.665
50MHz	2922	420.394	0.1434	0.318	0.318
100MHz	5174	400.254	0.0774	0.172	0.172

Looking at the first data point of BFW 10 transistor amplifier without feedback results of table 2, it shows that increases in operational frequency causes increases in gate source current (i_{GS}) while drain source currents (i_{DS}) are almost constant from 10Hz to 10kHz and starting decreases, these also causes the current gain (β), input impedance of transistor base(Z_{in}(base)), and input impedance decreases with increases in operational frequency**.** Also Looking at the first data point of amplifier with feedback results of table 3, it shows that increases in operational frequency causes increases in gate source current (i_{GS}) but with lower values compares with values without feedback, while drain source currents (i_{DS}) are almost constant from 10Hz to I MHz with higher values compares with ones without feedback and starting decreases, these also causes the current gain (β), input impedance of transistor base (Z_{in}(base)) and input impedance of BFW 10 transistor amplifier decreases with increases in operational frequencies but having higher values compares with ones without feedback. These characterized the BFW 10 transistor feedback amplifier having lower values of gate source current (i_{GS}), higher values drain source current(i_{DS}), current gain (β), input impedance of transistor base (Z_{in}(base)) and input impedance compares with BFW 10 transistor amplifier without feedback.

4.3. Effect of negative feedback on output impedance of BFW 10 transistor amplifier

At operating signals frequency of 10Hz, 100Hz 200Hz, 500 Hz, 1 KHz, 10 KHz, 1 MHz, 10 MHz, 20 MHz, 50 MHz, and100MHz, the effect of negative feedback on output impedance of BFW 10 transistor amplifier were calculated as shown in table 4 and 5.

Table 4: Output impedance calculated results of BFW 10 transistor amplifier without feedback

Operating signal frequencies	Gate source current (i_{GS})nA	Drain source current (i_{DS})nA	Current gain ($\beta = \frac{i_{DS}}{i_{GS}}$)	output impedance without Feedback Z_{in} K'Ω in
10Hz	0.095285	588.734	6178.664001	2.220162
100Hz	0.943778	598.613	634.2731	2.2215758
200Hz	1.885	597.714	317.0897	2.223152
500Hz	4.726	599.048	126.7558	2.2278851
I kHz	9.455	599.328	63.3874	2.2357679
10kHz	93.72	593.462	6.3323	2.2778396
100kHz	559.652	357.967	0.6340	3.7964785
IMHz	695.854	44.382	0.0638	17.8859467
10MHz	823.728	5.109	0.0062	162.427645
20MHz	1118	2.813	0.0025	402.01496
50MHz	2213	1.094	0.00049	2041.990204
100MHz	3790	0.415248	0.000109564	9124.626995

Table 5: Output impedance calculated results of BFW 10 transistor amplifier with feedback

Operating signal frequencies	Gate source current (i_{GS})nA	Drain source current (i_{DS})nA	Current gain ($\beta = \frac{i_{DS}}{i_{GS}}$)	output impedance without Feedback Z'_{in} K'Ω
10Hz	0.013478	738.367	54783.128	2.220018
100Hz	0.031899	745.498	23370.576	2.220043
200Hz	0.03907	745.183	19078.023	2.220052
500Hz	0.073294	745.855	10176.345	2.220098
I kHz	0.150122	745.912	4968.706	2.220201
10kHz	1.446	746.633	516.344	2.221934
100kHz	14.431	745.306	51.646	2.239338
I MHz	143.735	742.173	5.164	2.413405
10MHz	1069	579.526	0.542	4.0622703
20MHz	1497	447.459	0.299	5.560284
50MHz	2402	345.09	0.144	9.155729
100MHz	3791	293.249	0.106	11.642123

Comparing the output impedance calculated results of BFW 10 transistor amplifier with and without feedback of tables 3 and 4, shows that increases in frequency causes increases in output impedance of both amplifiers but amplifier with feedback has lower output impedance compares with one without feedback.

V. Conclusions

The BFW 10 n Channel JFET Single Stage Amplifier with and without feedback was designed and analyzed, the results compared proved that the BFW 10 n channel JFET Single Stage Amplifier with feedback had the advantages of Low-level Gain of 10.88db to 6.02db, Increased in Bandwidth from 10KHz to 1MHz, Controls in Distortion, Higher Input Impedance of 789.495kΏ to 0.172 kΏ and Lower Output Impedance 2.220018 kΏ to 11.642123 kΏ over BFW 10 n Channel JFET Single Stage Amplifier without feedback using Multisim 14.2 simulator.

References

[1]. Experts, D. (2019). *Guide to RRB Junior Engineer Stage II Electrical & Allied Engineering 3rd Edition*: Disha Publications.

[2]. Franklin, G. F., Powell, J. D., & Emami-Naeini, A. (2015). *Feedback control of dynamic systems*: Pearson London.

[3]. Fuada, S., Putra, A. P., Aska, Y., & Adiono, T. (2016). *Trans-impedance amplifier (HA) design for Visible Light Communication (VLC) using commercially available OP-AMP.* Paper presented at the 2016 3rd International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE).

[4]. Mehta,V.K., & Mehta, R. (2008). *Principles of Electronics, Revised Eleventh Edition. S. Chand* & company LTD, India,ISBN: 81-219-2450-2.

[5]. Navas, K. A., & Suhail, T. A. (2010). *Basics of Electrical Electronics and Communication Engineering: Conceptual Approach*: RAJATH PUBLISHERS.

[6]. Piguet, C. (2018). *Low-Power Electronics Design*: CRC Press.

[7]. Rao, B. V. (2012). *Electronic Circuit Analysis*: Pearson.

[8]. Sikder, M. S., & Ali, M. T. (2021). *Performance analysis of High Frequency Class E Feedback amplifier with Schmitt Trigger driver.* Paper presented at the 2021 2nd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST).

[9]. Singh, R., & Mehra, R. (2018). Qualitative Analysis of Darlington Feedback Amplifier at 45nm Technology. *Bulletin of Electrical Engineering and Informatics, 7*(1), 21-27.

[10]. Zanjani, S. M. A., Dousti, M., & Dolatshahi, M. (2018). High-precision, resistor less gas pressure sensor and instrumentation amplifier in CNT technology. *AEU-International Journal of Electronics and Communications, 93*, 325-336.